JEDEC PUBLICATION

Guideline for Evaluating Gate Switching Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion

JEP195

FEBRUARY 2023

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GUIDELINE FOR EVALUATING GATE SWITCHING INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION

Contents

Foreword

This publication has been drafted and approved by the JEDEC JC-70.2 SiC Power Electronic Conversion Semiconductor Standards subcommittee, which consists of recognized industry experts from foundries and fabless member companies.

While the existing JEDEC document JEP184 “GUIDELINE FOR EVALUATING BIAS TEMPERATURE INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION” addresses the bias temperature instability and related static gate stress, this document addresses more application-oriented gate stress testing and how to quantify the silicon carbide specific degradation mechanisms of gate switching instability.

Introduction

The objective of this publication is to help to further extend the information given by JEP184 regarding the long-time stability of parameters like threshold voltage not only under static conditions but also under application near switching conditions. Under such conditions a SiC specific degradation mechanism called “gate switching instability” can occur including drift values that can exceed the drifts seen under static conditions. After describing the mechanism and the influencing factors this guideline suggests a test procedure called “gate switching stress test”. The aim of this test procedure is to evaluate the drift that has to be expected in the application for a device technology.

GUIDELINE FOR EVALUATING GATE SWITCHING INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION

(From JEDEC Board Ballot JCB-22-62, formulated under the cognizance of JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee.)

1 Scope

The scope of this document covers SiC-based PECS having a gate dielectric region biased to turn devices on and off. This document should enable the reader to evaluate the consequences of SiC MOSFET specific parametric drift mechanism called “gate switching instability” for the device and/or the application. Additionally, the gate switching stress (GSS) test is described, enabling the calculation/measurement of the worst-case drift that has to be anticipated until the end of the application profile

2 Normative References

JEDEC JEP183, Guidelines for measuring the threshold voltage (VT) of SiC MOSFETs, 2021.

JEDEC JEP184, Guideline for Evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion, 2021.

3 Terms and Definitions

Terms that are already defined in JEP184 are only listed if something relevant for this document is added. For the missing definitions, consolidate JEP183 and JEP184.

Gate switching instability (GSI): threshold voltage instability of a MOS device operating in a gate switching mode between a voltage much above the threshold voltage and below the flatband voltage. Generally, describes the degradation in the conduction path of the device driven by the switching event.

Gate switching stress (GSS): Stress test to measure the GSI-induced degradation under simplified switching conditions.

Frequency (f): switching frequency of the SiC MOSFET

Number of switching cycles (N_{cycles}): number of switching cycles between gate and source calculated by multiplying the time under operation with the frequency: $N_{cycles} = t \times f$.

End of application profile (EoAP): assumed end point in time of a given application profile.

3 Terms and Definitions (cont'd)

Number of switching cycles until end of application profile (N_{cycles}^{EoAp}): Number of switching cycles between gate and source at the assumed end of the application profile.

Critical negative gate voltage (V_{GS}^{crit}): for V_{GS} values lower than V_{GS}^{crit} significant GSI effects are observed. Typically, V_{GS}^{crit} is below the flatband voltage of a device. V_{GS}^{crit} is strongly depended on the device technology.

Gate-source voltage including overshoots (V_{GS}^{OS}): maximum V_{GS} occurring in operation including overshoots.

Gate-source voltage including undershoot (V_{GS}^{US}): minimum V_{GS} occurring in operation including overshoots.

Maximum gate-source voltage (V_{GS}^{max}): Maximum gate-source voltage recommended for a device, for any time period during operation (as given in the datasheet).

Minimum gate-source voltage (V_{GS}^{min}): Minimum gate-source voltage recommended for a device, for any time period during operation (as given in the datasheet).

Gate-source voltage recommended operating value (V_{GS}^{on}): recommended gate-source voltages during normal on-state.

Gate-source voltage recommended operating value (V_{GS}^{off}): recommended gate-source voltages during normal off-state.

Bias temperature instability (BTI): susceptibility of the threshold voltage of an MOS device to change over time under bias and temperature stress. It is used generally to describe MOS-based transistor threshold stability under both gate voltage and temperature stress and is described further in JEP184.

Threshold voltage at a given stress time ($V_{Tt\#}$): the V_T is measured over time during the BTI or GSS test, thus a time-related subscript can be used when referring to a particular stress time. For improved extrapolation of V_T over time, the initial measured V_T during BTI or GSS should be after a brief (~100ms) initial stress and/or conditioning, such that V_T (or V_{Tt0}) occurs after the initial brief stress. The initial pre-stress V_T and the final post-stress V_T may be defined using different subscripts, such as V_{Tpre} and V_{Tpost}, respectively.

Threshold voltage shift (ΔV_T^{shift}): a change in the measured V_T value from an initial to a final condition, here particularly focused on the V_T shift during BTI or GSI stress. This shift is described as the ongoing shift over time ($V_{Tt\#}$ - V_{Ti}), which by the end of the test would be the final V_{Tf} minus the initial V_{Ti}. This shift value could be due to: 1) transient charging effects (ΔV_T^{trans}) which are fully recoverable, 2) transient effects which have a permanent component (ΔV_T^{hyst}), or 3) permanent (non-transient) interface effects (ΔV_T^{drift}). More generally, V_T shift is the change in V_T between any two measured values, and can arise from a change in gate bias, or the continued application of the same gate bias.

3 Terms and Definitions (cont'd)

Threshold voltage drift (ΔV_T^{drift}): describes GSI or BTI induced changes in V_T (ΔV_T^{shift}) which are relatively permanent, after transient V_T recovery effects are removed. For example, if a V_T^{shift} is measured without a change in transient effects, there would be a shift in the voltage location of the threshold voltage due only to a ΔV_T^{drift} effect; the measured hysteresis (V_T^{hyst}) would remain unchanged. As most parts of the drift for GSI are not recoverable, there is most times not a big difference between ΔV_T^{drift} and ΔV_T^{shift} for GSI (in contrast to BTI).

Threshold voltage transient shift (ΔV_T^{trans}): portion of the BTI threshold shift (ΔV_T^{shift}) that quickly recovers after removal of gate stress. For BTI, this is typically larger or beyond what a short hysteresis measurement would reveal, due to time at bias effects during BTI that result in charging on a time scale that a short hysteresis measurement does not capture. This transient portion may contain changes in hysteresis (ΔV_T^{hyst}), besides other more slowly varying transient components. Changes in the hysteresis may be able to be isolated from the other transient effects, depending on the BTI test method. In contrast to BTI, this is, according to the current literature, not changing due to GSI.

4 General Introduction to the Degradation Mechanism Gate Switching Instability

Based on years of experience in silicon (Si) technology, the long-time stability of Si devices in regards to gate oxide driven degradation mechanisms like BTI is typically addressed by static tests, such as HTGB. This is also valid for silicon carbide and described in JEP184. Besides these well-known mechanisms and the corresponding reliability tests, a separate, but possibly related mechanism causing long-term parameter instability has been found in recent years [1, 2, 3]. In contrast to BTI, this new mechanism is not driven by static gate voltage stress but by the switching events themselves. Furthermore, the dependence on the stress temperature is not necessarily comparable to the one of BTI. Due to this the degradation mechanism is called gate switching instability (GSI).

There are publications aiming to empirically explain the key experimental observations as a result of GSI. The common aspect of existing models is that fast switching traps at the SiC/SiO_2 interface likely play a major role in GSI:

- **Local field enhancement**: During the high and low phases of the gate pulse charges may get trapped at the gate oxide/SiC interface. Some of these charges remain trapped during fast the transition phases of the gate voltage thereby enhancing the oxide electric field during and shortly after the gate switching event. This enhanced field may trigger a stronger V_{th}-drift under bipolar gate switching conditions [4-6].
- **Recombination**: Due to bipolar gate switching electrons and holes can recombine at the MOS interface thereby releasing recombination energy in every single switching cycle. The energy is assumed to be released mostly through vibrational excitations and partly through radiation. The released energy can act as a "phonon kick" to break a nearby bond or to bring a defect to an excited vibrational state from which it can experience a reaction into a charged state [6].

4 General Introduction to the Degradation Mechanism Gate Switching Instability (cont'd)

The complete phenomenon might be a combination of both effects. Further studies will contribute to a more complete description of GSI. As such a complete description is not available yet, the influence of various parameters and observations from literature are used to describe the effect:

- By switching the device between gate voltage much above the threshold voltage and below the flatband voltage, a threshold voltage drift ΔV_T^{drift} is introduced. This ΔV_T^{drift} can exceed the drift seen in typical BTI experiments performed at similar but static gate bias levels and temperatures [1, 2, 7, 8].
- The applied V_{DS} plays, according to current literature, no role in the degradation [9, 10]. As the physical root cause of the mechanism is not fully understood, this has to be verified for different technologies and vendors.
- GSI-induced threshold voltage drift is typically positive, meaning the V_T increases during stress.
- GSI is caused by the switching event and is independent of the duty cycle over a wide range [7]. Therefore, the relevant parameter to describe the evolution of the degradation is not the time under stress but the number of switching events [1, 7, 11], Similar to BTI, the evolution of the degradation can be described by a power law, such as:

$$\Delta V_T = a\, N_{cycles}{}^{b} \qquad (1)$$

but including N_{cycles} instead of the time under stress.

According to the literature, GSI might be a superposition of different degradation mechanisms and thereby may show different power law exponents *b* during a long-term stress experiment. Refer to Figure 1 [3, 10].

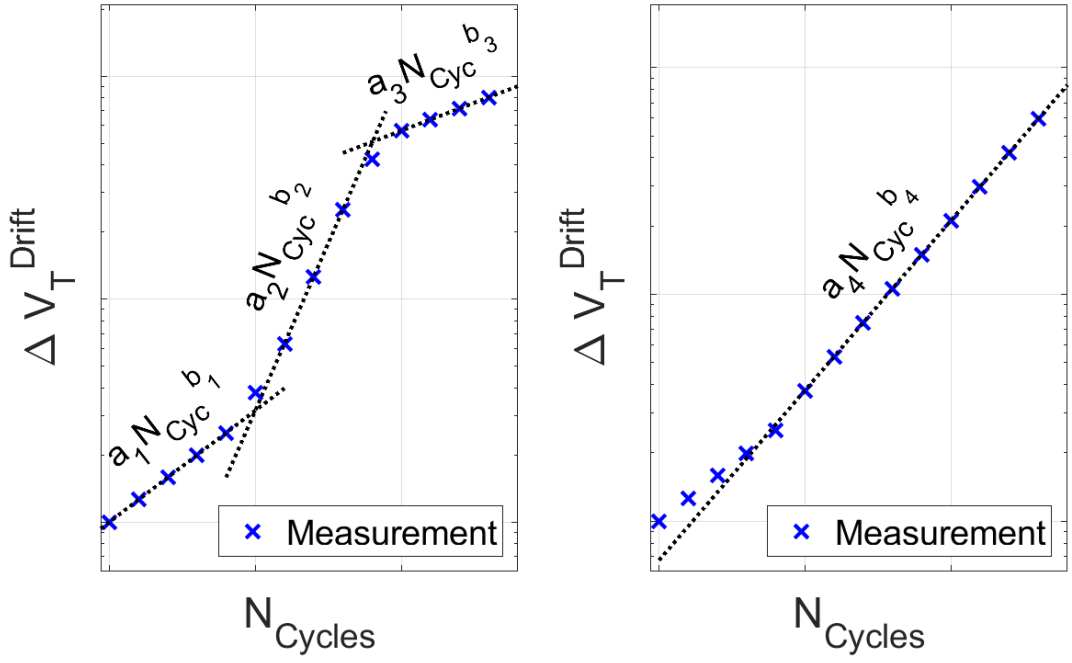


Figure 1 — Exemplary Plot of GSI-Induced V_T Degradation as a Superposition of Multiple Power Laws

4 General Introduction to the Degradation Mechanism Gate Switching Instability (cont'd)

- The drift of V_T leads (due to a reduced overdrive) to a drift in $R_{DS(on)}$ [10]. Also, for some devices there are hints that a degradation of the channel mobility may be present in addition as the change in $R_{DS(on)}$ can in some cases be larger than the change that would be expected due to the ΔV_T^{drift} only [7].
- There are no hints that leakage currents (neither drain-source nor gate-source) are affected by GSI.
- Up to now it has not been observed that the drift depends on the switching frequency, current reports go up to 2 MHz [11]. In the high frequency limit an influence has certainly to be expected due to impedance of the test hardware or a not homogenous turn on / off of a MOSFET.
- It is necessary to switch the device off using a sufficiently low negative gate voltage [1, 7, 8], referenced to as critical negative bias V_{GS}^{crit}. If V_{GS}^{off} is above this critical voltage, the V_T degradation can be described as a superposition of negative and positive static BTI without ever showing V_T drifts that exceed the values of BTI (see JEP184). If the V_{GS} is below this V_{GS}^{crit}, GSI may become the dominant degradation mechanism depending on stress conditions and number of cycles leading eventually to higher V_T drifts as compared to BTI. This V_{GS}^{crit} is device and technology depended [1, 7, 8].
- If V_{GS}^{off} is below V_{GS}^{crit}, lower turn off voltage leads to higher ΔV_T^{drift}. For some devices a saturation effect can be observed at very low turn off voltages so that a further decrease of V_{GS}^{off} does not lead to more ΔV_T^{drift} [7].
- Higher turn on voltages also lead to an increased degradation and thereby to a higher ΔV_T^{drift} [1, 7, 8].
- Over and undershoots of the gate voltage levels have a strong influence on GSI-induced ΔV_T^{drift} level. As described before, the drift depends on the maximum and minimum gate voltage between which the devices are switched. This includes over- (V_{GS}^{OS}) or undershoots (V_{GS}^{US}) that might be present in the system [1, 7] as these lead to a similar degradation as if the device was switched to the level of the over/undershoot continuously. This is different to other gate oxide failure mechanisms where only the time the voltage is applied is relevant.
- The role of temperature on the degradation is today not consistent across devices from different manufactures. For most devices, the literature reports that a lower temperature leads to a higher ΔV_T^{drift} in a temperature range between room temperature and the maximum junction temperature [2, 7, 8]. At least some reports indicate that, however, the ΔV_T^{drift} can also increase with increasing temperature [1].
  - The GSI-induced effects seem to be quasi-permanent and does not show significant relaxation within typical recovery times between stress and measurement. This is in contrast to BTI where often a strong recovery of the ΔV_T^{shift} is seen after stress [3, 7]. Consequently, this document neglects changes in V_T^{trans} and focusses on V_T^{drift} and $R_{DS(on)}^{drift}$ instead of $R_{DS(on)}^{shift}$ and V_T^{shift}.
  - The speed of switching/the slope influences the degradation, faster switching leads to higher drift values in some cases [4, 8].

5 Gate Switching Stress to Measure GSI-Induced Drifts

Current reliability tests are not addressing GSI as they are conventionally performed under static conditions. To address GSI, a reliability test that focusses on switching the device between different gate-source voltage levels has to be performed. In the following, such a gate switching stress procedure is described aiming to trigger similar degradation as it would also appear in typical switching applications of SiC MOSFETs. The gate is stressed against drain/source (while keeping drain/source shortened) by applying an alternating gate voltage. In the absence of a universally valid degradation model, it is recommended to stress devices under worst case gate bias and temperature conditions to ensure that the datasheet is covered by the stress test:

- **V_{GS}:** The device should be stressed with the minimum (V_{GS}^{min}) and maximum (V_{GS}^{max}) gate source voltages to include all effects that can occur in the application, also over- and undershoots. An illustration of the different relevant voltage levels is given in Figure 2. As GSI depends on the switching and not on the duty cycle, possible extensions of the nominal datasheet range covering short time over- and undershoots have to be included into this consideration [7]. Performing the stress only between recommended V_{GS}^{on} and V_{GS}^{off} is not sufficient, as the over and undershoot are allowed in the whole datasheet range. To neglect even small differences caused by different duty cycles and enable better comparability of the stress test result, a duty cycle during stress reduced by 50% is recommended.
- **$T_{vj,stress}$:** Devices should be stressed at worst case application conditions, the temperature range to be considered during stress is therefor between room temperature (typically 25°C) and $T_{vj,max}$. Lower temperatures are excluded as self-heating is expected to heat up the devices at least to 25°C. As outlined before, the worst-case value of this stress parameter can differ strongly between the different chip technologies and has to be chosen with care.
- **Waveform:** The switching curve should be of trapezoidal shape and designed in a way that the above defined gate voltages are reached without significant over-/undershoots (<0.5 V). This enables comparability between different stress conditions/test benches etc. without being influenced by duration or height of any over- or undershoot, an example is given in Figure 2. The influence of other parameters like voltage slope should be covered by designing the testbench in a way that switching curves reassemble fastest switching curves from typical device applications as indicated in Figure 2**Error! Reference source not found.**. Switching the gate much faster than in typical applications is not recommended since over- and undershoots may become increasingly hard to control at high dV_{GS}/dt. This can also result in drift values much higher than occurring in the application as the slope also influences the drift. Because of this, the slope should not be smaller than in the application. Typical values for fast applications are around 0.1 V/ns to 0.3 V/ns and can be used for GSS-testing.
- **Stress frequency:** High switching frequencies can be used to accelerate degradation. Today, all frequencies up to 2 MHz are reported to result in the same degradation after the same number of switching events [11]. At higher frequencies one has to take particular care that the whole chip can be still switched on and off during the respective phase of stress. Most stress tests given in the literature are performed at frequencies up to 500 kHz due to this.

5 Gate Switching Stress to Measure GSI-Induced Drifts (cont'd)

Please note that the parameters are only meant as a guideline for typical worst-case conditions based on today's literature. If vendors find that for their device other conditions within the allowed datasheet range are leading to more degradation than the ones described above, these conditions should be chosen for GSS.

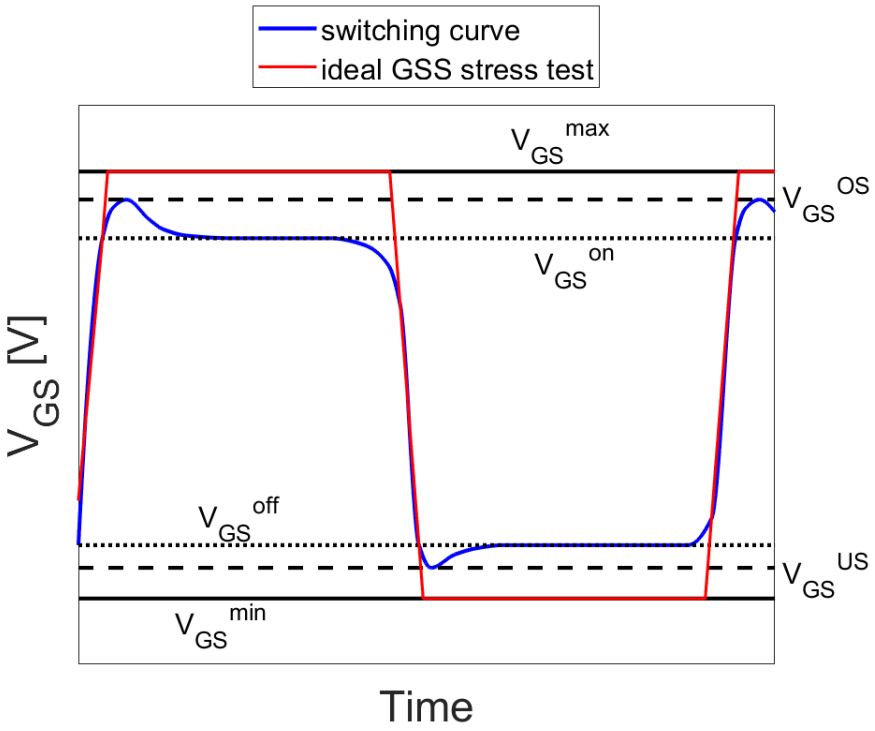


Figure 2 — Schematics to Explain the Definition of Different Voltage Levels

The stress duration of the GSS test depends on the stress frequency and on the total number of switching cycles until end of application profile (EoAP). For applications that exhibit relatively small numbers of switching events (e.g., $< 10^{12}$), the total number of cycles until EoAP can be reached after some 100 h when using, for instance, a stress frequency of 500 kHz. If the number of cycles until EoAP is much higher (e.g., $> 10^{13}$), it is not feasible to reach the total number of cycles until EoAP within a reasonable time frame using 500 kHz stress frequency. In this case, the GSS-test should at least be performed until the equivalent of a 1000 h test at 500 kHz (meaning 1.8×10^{12} cycles). The evaluation of the drift until EoAP can then be estimated by extrapolation as explained in chapter 6.

5 Gate Switching Stress to Measure GSI-Induced Drifts (cont'd)

To validate the evaluation of the GSI-induced parameter drift, it is recommended to perform multiple readouts during a GSS with logarithmically increasing time periods in-between. Initially, intermediate and final V_T-measurements should be done using conditioning pulses as described in JEP184 document. To measure V_T^{UP} and V_T^{DOWN} in order to calculate V_T^{HYST}, it is recommended to use positive and negative conditioning pulses in the readout sequence as defined in JEP183 and JEP184. Since the degradation due to GSS is reported to be relatively stable over time without showing much of recovery after terminating stress, the time delay between end of stress and readout is not as critical as for DC BTI, c.f. JEP184. Thus, it is allowed to let device cool down and measure them sequentially during intermediate and final readouts. The cool down and measurement procedure should, however, not be unnecessarily long and always much shorter than the preceding stress time.

During a readout, it is recommended to measure all relevant electrical device parameters that may show degradation due to GSS, e.g., V_T, V_T^{HYST}, $R_{DS(on)}$ and leakage currents (I_{DS}; I_{GS}). If measuring all relevant electrical device parameters is not possible by intermediate readouts, e.g., due to limitations of the test bench, the entire set of relevant electrical device parameters has to be evaluated at least in the initial and final readout so that total drifts of all parameters are available and can be reported. In order to monitor and later extrapolate the evolution of degradation during GSS, it is recommended to record at least the drift in V_T by intermediate readouts. Readouts may be performed either at stress temperature or at room temperature, as it is reported that this does not influence the measured ΔV_T [3] . Of course, all readouts have to be performed at the same temperature.

6 Evaluation of GSS Results

The target of a GSS test is to estimate the worst-case drift of critical electrical device parameters at the end of an arbitrary application profile to enable customers to calculate safety margins in their system design. Guidelines to achieve that are described in this chapter.

6.1 Number of Cycles Until End of Application Profile Reached Within GSS Time

If the number of cycles until end of application profile is reached within the test duration, the drift until end of application profile for all parameters can be estimated from intermediate and/or final readouts. Once the test exceeds the maximum number of required switching cycles one may either interpolate between intermediate readouts or take the first readout after exceeding the required number of switching cycles as final readout for this application. Due to this, it is possible to reference GSI results from one device technology to multiple application profiles.

If one is not interested in the drift under worst-case data-sheet conditions but more in the drift under some predefined customer specific application conditions, vendors may perform GSI tests under any desired gate bias and temperature conditions and report the result after a certain number of switching cycles as a case study. Also, in this case, the application specific over and undershoots have to be considered (cf. Figure 2) by stressing at V_{GS}^{max} and V_{GS}^{min}. The drift result would then correspond to the exact drift that has to be expected in the application for these particular stress conditions. As described in chapter 4, the GSI mechanism is a superposition of multiple degradation mechanisms, therefor this is only a suitable approach if the $N_{\mathbf{cycles}}$ reached in GSS is higher than or equal to N_{cycles}^{EoAp}.

6.2 Number of Cycles Until End of Application Profile Not Reached Within GSS Time

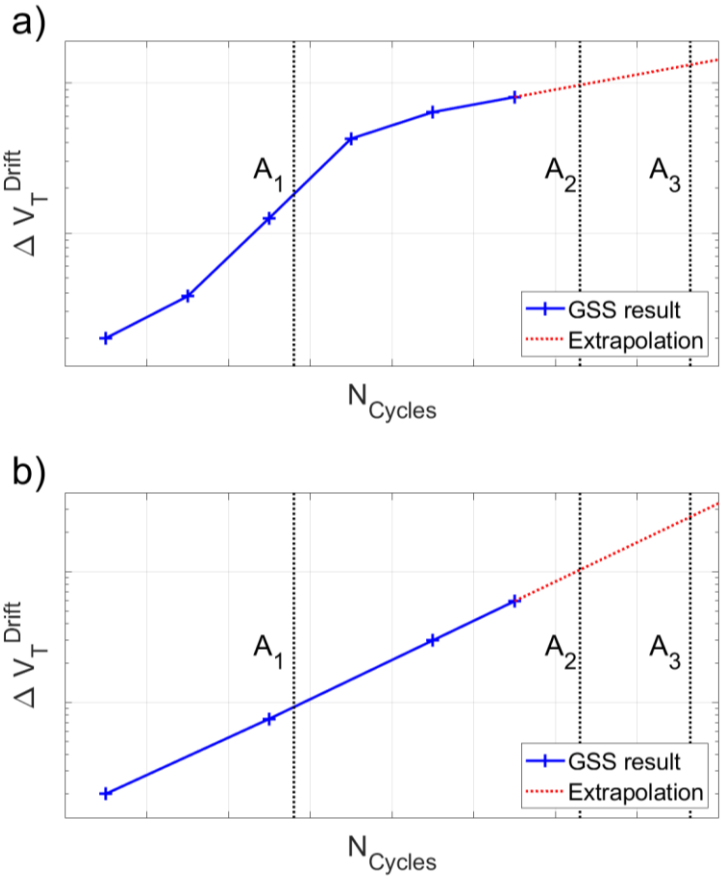
If the number of cycles until EoAP cannot be reached within a reasonable stress time, typically 1000 hrs with a frequency up to 500 kHz, a different approach is proposed to estimate the drift until EoAP. It has been demonstrated in literature that extrapolation of drift results from a 1000 hrs test may yield reasonable and realistic worst-case results for EoAP that exceed the actually tested number of switching cycles by more than one order of magnitude [3,10].

However, since the observed drift can be a combination of different power laws as shown in Figure 1, an extrapolation toward EoAP is only valid when it is ensured that the power law exponent has settled or at least will not increase anymore beyond the tested number of switching cycles. If this is not the case, the extrapolation of the drift may underestimate the worst-case drift. It has to be ensured for every technology that this condition is valid for the data points that are used for the extrapolation e.g., by feasibility tests running as close as possible to the actual EoAP according to reasonable experimental constraints. An extrapolation approach is outlined in this subchapter.

6.2 Number of Cycles Until End of Application Profile Not Reached Within GSS Time (cont'd)

To calculate the power law factors for the extrapolation all data points from the same power law regime can be used (compare equation (1) and Figure 1). For extrapolation the last two datapoints are most important as they represent best the drift regime beyond the measured data points. Also, the distance in time between the datapoints that are used for extrapolation should be large enough to allow a reasonable data fit, e.g., 500 hrs and 1000 hrs or 1 to 2×10^{12} switching cycles. Since the maximum test time is not limited, a test can always be prolonged beyond 1000 hrs to get closer to EoAP and hence achieve a more reliable extrapolation result. Figure 3 shows two possible ways how a GSS-result might look for a GSI-induced degradation as given in Figure 1. The vertical lines indicate the N_{cycles}^{EoAp} for different applications (A_1, A_2, A_3) showing that the ΔV_T^{drift} depends strongly on the N_{cycles}^{EoAp}.

Estimating the $\Delta R_{DS(on)}^{drift}$ until EoAP from a GSI test can be challenging since the $\Delta R_{DS(on)}^{drift}$ may not only depend the ΔV_T^{drift} but can also be affected by additional changes in the channel mobility. As there are literature references showing only ΔV_T^{drift} depended $\Delta R_{DS(on)}^{drift}$ [3, 10], but also references showing an additional $\Delta R_{DS(on)}^{drift}$ [7] due to mobility degradation, vendors have to verify that the chosen extrapolation approach reassembles correctly the device behavior until EoAP.



NOTE a) For a device with multiple power laws. b) For a device with a more simplified drift behavior. The application relevant V_T drift depends on the number of cycles in different applications, three different ones are given as A_1, A_2 and A_3.

Figure 3 — Two Different Results from GSS Tests

6.2 Number of Cycles Until End of Application Profile Not Reached Within GSS Time (cont'd)

Two ways are possible:

- **$R_{DS(on)}$ drift is caused only by V_T variation:** The $\Delta R_{DS(on)}{}^{drift}$ is due to $\Delta V_T{}^{drift}$, and hence, can be calculated directly from the $\Delta V_T{}^{drift}$. To calculate the $\Delta R_{DS(on)}{}^{drift}$, devices need to be characterized before stress at different temperatures and V_{GS} around $V_{GS}{}^{on}$: $R_{DS(on)}$ (V_{GS}, T_{vj}). With the $\Delta V_T{}^{drift}$ data obtained during GSS, these $R_{DS(on)}$ (V_{GS}, T_{vj}) measurements can then be used to calculate $\Delta R_{DS(on)}{}^{drift}$ ($V_{GS}{}^{on}$ - $\Delta V_T{}^{drift}$, T_{vj}). With this approach, even $\Delta R_{DS(on)}{}^{drift}$ for different junction temperatures can be calculated in a straightforward manner from the $\Delta V_T{}^{drift}$. This enables to calculate the $\Delta R_{DS(on)}{}^{drift}$ and thereby the safety margins for various N_{cycles} and temperatures based on one GSS-test result. It is recommended to verify this simplified approach for $\Delta R_{DS(on)}{}^{drift}$ estimation for each technology at least by measuring the $\Delta R_{DS(on)}{}^{drift}$ due to GSI in the last readout and compare it to the $\Delta R_{DS(on)}{}^{drift}$ calculated from the $\Delta V_T{}^{drift}$.

  The big advantage of this simplified approach is that the $R_{DS(on)}$ does not need to be tracked in intermediate readouts which reduces testing efforts, minimizes error sources due to limited measurement resolution and allows for more flexible referencing of drift data to similar products of the same device technology. Note that as opposed to the $\Delta R_{DS(on)}{}^{drift}$ the $\Delta V_T{}^{drift}$ is typically independent of measurement temperature and chip size. If it turns out that the $R_{DS(on)}$ cannot be explained by the $\Delta V_T{}^{drift}$ alone, another approach has to be chosen.

- **$\Delta R_{DS(on)}{}^{drift}$ is caused by $\Delta V_T{}^{drift}$ and other mechanisms like channel mobility degradation:** If the comparison of the measured and the calculated $\Delta R_{DS(on)}{}^{drift}$ shows significant differences, further degradation mechanisms that affect, for instance, the channel mobility, are also present. In this case one has to measure $\Delta R_{DS(on)}{}^{drift}$ in addition to $\Delta V_T{}^{drift}$ throughout the experiment maybe also at different temperatures. Due to this, the flexibility of referencing $\Delta R_{DS(on)}{}^{drift}$ data across similar products and temperatures is lost. Nevertheless, the approach is particular useful and straightforward if the number of cycles is reached within the stress time. If not, one has to use a similar power law extrapolation approach as recommended for the $\Delta V_T{}^{drift}$. The extrapolation is then, however, much more complicated as the $\Delta R_{DS(on)}{}^{drift}$ is then a superposition of different effects with a possibly different time evolution. Due to this, verifying the approach by tests until EoAP with very long runtimes is mandatory. Consequently, the first approach is preferred, however, eventually vendors have to prove that the approach they use is appropriate to correctly estimate the $\Delta R_{DS(on)}{}^{drift}$ until EoAP.

Additional to the evaluation of $\Delta V_T{}^{drift}$ and $\Delta R_{DS(on)}{}^{drift}$, further measurements are recommended to ensure that the devices are not affected in any other imaginable way due to the GSI mechanism. It is suggested, for example, to compare at least exemplary switching behavior and switching losses before and after GSS, also it has to be ensured that parameters like I_{DSS}, I_{GS} and V_{hyst} are unchanged and still within the limits applied for a device qualification.

7 Considering GSI for Application Safety Margins

This chapter gives a proposal for how to communicate the application relevant GSI-induced drift results.

The relevance of GSS test results for the application is only valid if it is proven that the drift is also observed in the range of application near conditions. Up to now, there are no reports showing the opposite, but there are examples where the drift in an application test and GSS show good agreement up to higher numbers of cycles [9, 10]. The calculated drift depends strongly on the device end-use application. A customer using the device only in an automotive drive train with a normal EoAP of ~10^{12} cycles or less will experience a smaller drift compared to, for example, a long running automotive application or a solar application that is being continuously switched for 20 years or more (see Figure 3).

Because of this, it is suggested that vendors communicate the dependency of the drift on the application profile or N_{cycles} to the customer. In particular, if the drift may cause violations of spec limits at the EoAP. As GSS is reflecting the drift during switching of the device, the EoAP drift result reflects all application relevant gate oxide trapping and further degradation mechanisms for SiC switches, enabling customers to define the correct safety margins for SiC MOSFETs even if, until now, not all physical mechanisms are understood. With this information, customers can use this drift in their calculations to ensure margin for a reliable device function until EoAP.

8 Bibliography

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